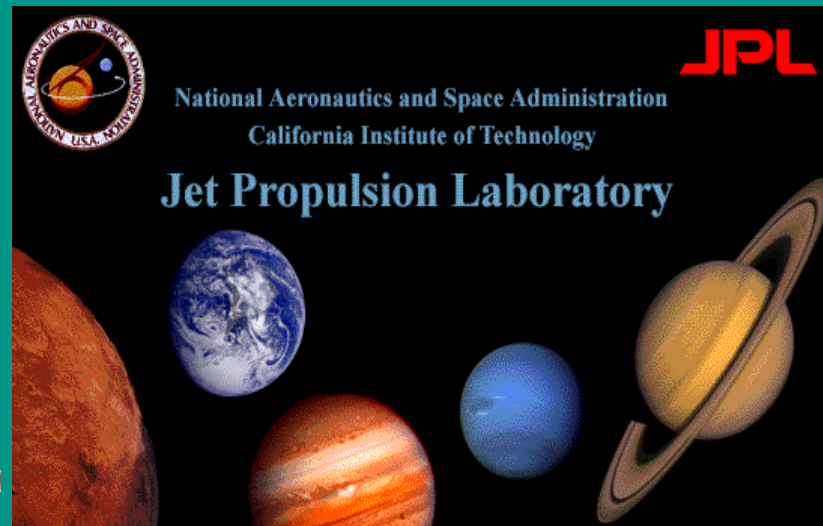
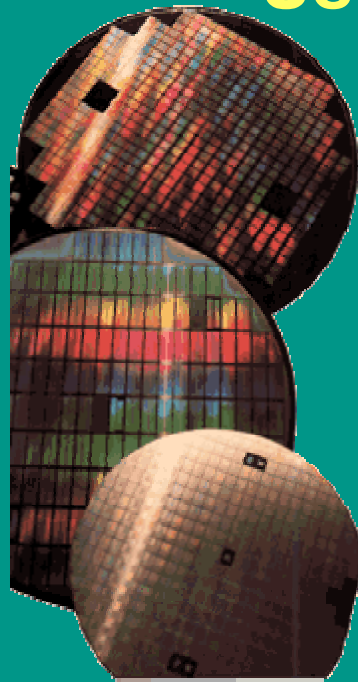


Electronic Packaging Workshop for Space Applications

1998

Commercial Off-The-Shelf (COTS)
Parts/Technology Program

**Avoiding Risks When
Using Known-Good-Die**



Mike Sandor & Shri Agarwal

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The COTS Program Initiative:

Develop a *methodology* to evaluate & select COTS that-

- Minimizes the cost of part risk management
- Uses an engineering-based approach vs “rule’ based
- Stimulates gaining new knowledge and experience
- Establishes a systematic approach to evaluation
- Uses Mfr. and other pre-existing data as much as possible
- Provides optimized evaluation & test path per part
- Allows trade-off assessment with high reliability parts
- Establishes COTS guidelines for JPL Space Applications



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WHAT IS THE MEANING OF COTS ?

COTS are parts (die) whose specification is manufacturer-controlled as opposed to traditional “Hi-Rel” parts whose specification was Government or customer-controlled

LEVELS OF RISK FOR COTS PARTS:

LEVEL 1 - Part (die) procured and used as is from vendor or distributor. Risk to JPL is unknown and no recommendation can be made for 1st time use.

LEVEL 2 - Part (die) procured and used after JPL recommended minimum evaluation and acceptance. Risk to JPL is moderate and a recommendation can be made.

LEVEL 3 - Part (die) procured and used after JPL extended evaluation, characterization, and acceptance. Risk to JPL is low and recommendation is made with high confidence.

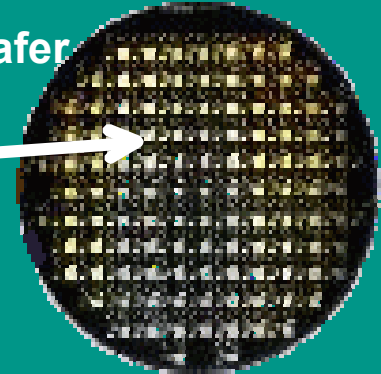


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Known-Good-Die (KGD)

Bare Wafer



Definition:

A Known-Good-Die is an unpackaged die (chip) characterized to the highest quality, reliability, and performance level as a packaged die.

Minimum Tested Die (Bare Die)

Definition:

A bare die is minimally tested to eliminate most gross failures.



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KGD Issues Relevant to JPL Space Applications:

Vendor liability may be less

Test strategies, ETS, Q/R are wide open

Procurement procedures are not defined

Upscreening is not defined (if needed)

No procedures for handling and storing of die

No methodology for programming KGD (PLDs)

Little yield data on KGD integration with assemblies



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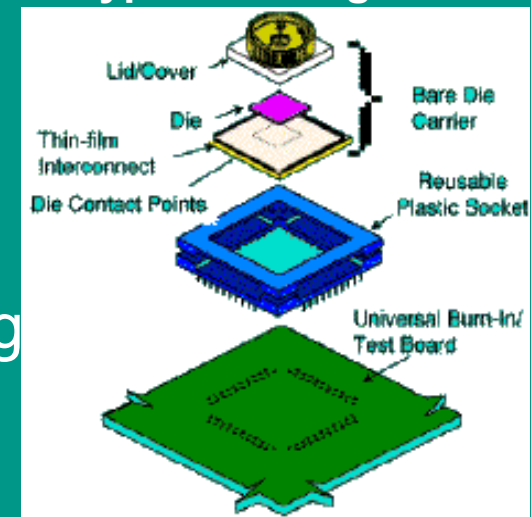
Unresolved Issues

A. The KGD JEDEC specification has not been accepted

B. JPL has not adopted any KGD carrier technology used for:

1. Electrical Testing, Burn-In, etc.
2. Radiation Evaluation and Testing

Typical Configuration



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KGD Current Activities:

Performing vendor surveys to compare KGD programs and the multiple options within

Evaluating the value added of these various options

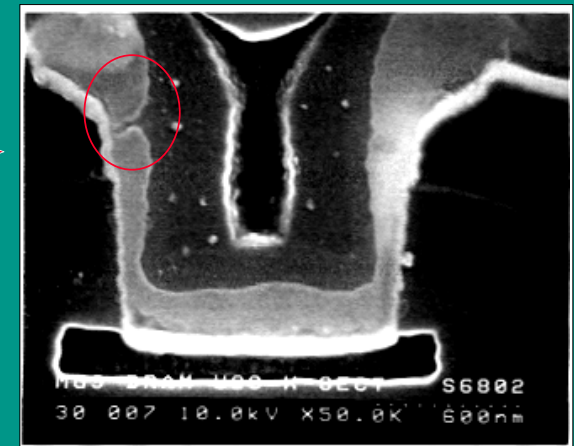
Evaluating KGD criteria for screening, shipping, documentation, etc.

Negotiating obtaining RH KGD

Construction Analysis 

Providing information and services to users

DRAM DIE Contact



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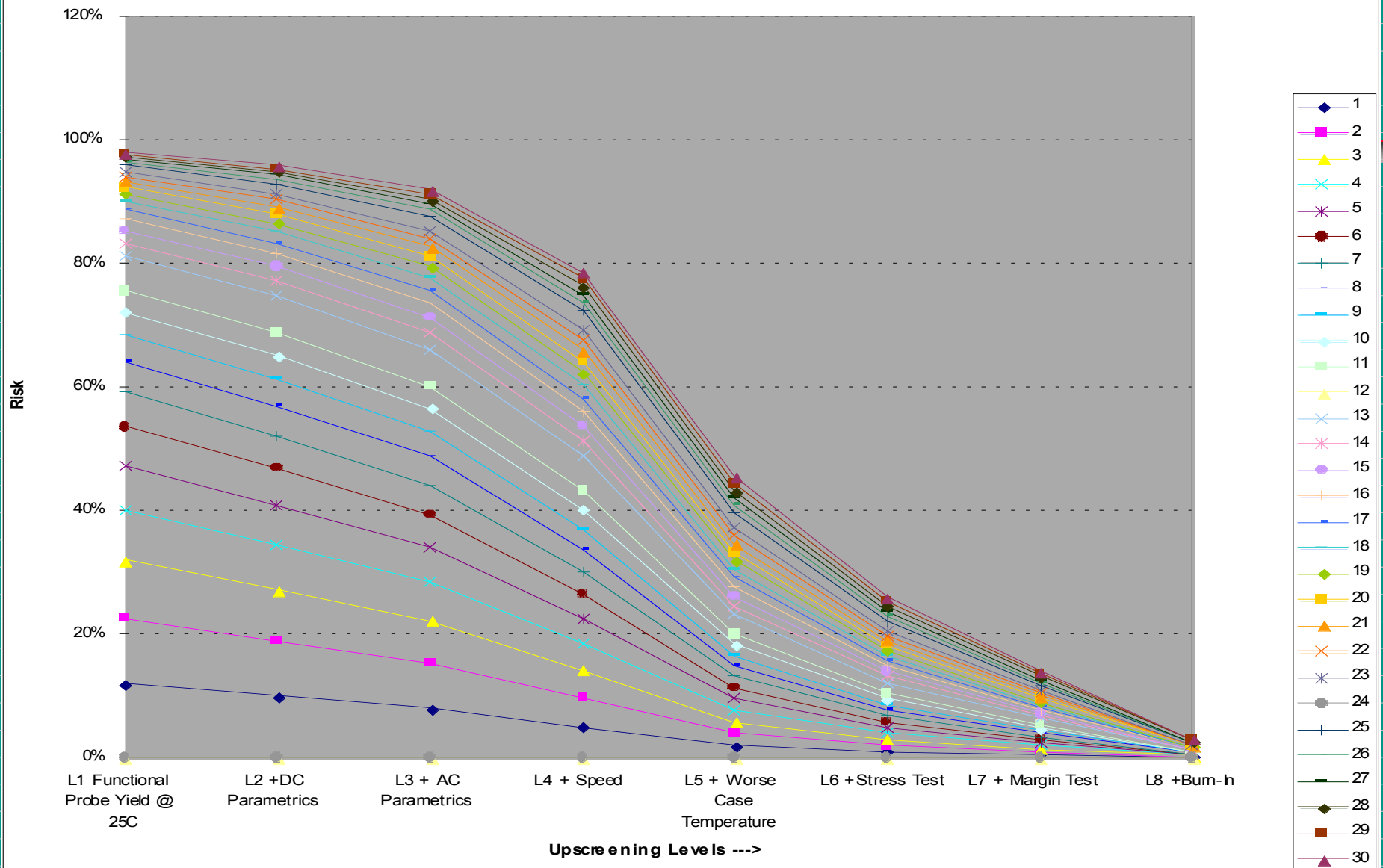
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Assumptions For Ascertaining MCM Risk of Failure

- $\text{MCM Yield (with die)} = \text{KGD yield}_{\text{Vendor A}}^{\wedge \text{No. of die Vendor A}} \times \dots\dots\dots$
- A MCM yield of 1.0 means the die are tested to the highest level as the package part for quality, reliability, and performance ➡ (KGM)
- The MCM substrate yield (w/o die) is assumed equal to 1.0
- Vendors who supply KGD offer many screening options
- Rework of MCMs due to faulty die is costly, hard to trouble shoot, and causes delay in schedules - it should be avoided



MCM Risk of Failure vs Upscreening Levels



Note: Assume KGD Die Yield_{Vendor A} = 88 % for L1 bare die
L1 yield can be as low as 70% for non-mature products.

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KGD Module Yield Vs. Die Quality (Actual Case - Courtesy of National Semiconductor)

Example 1: Dual Processors with on-board memory & self test

- MCM with 32 ICs assembled w/o KGD (.85 avg. yield)
- First Time : Zero
- Reworked Yield: 100%
- Averaged 3 IC replacements/MCM

Example 2: DSP capable of 400 million floating point operation/s

- MCM with 57 ICs assembled using KGD (.99 avg. yield)
- First Time Yield: 58%
- Reworked Yield: 100%
- Averaged 0.5 IC replacements/MCM
- IC replacements
 - zero % of processors
 - zero % of ASIC
 - 1% of memory chips



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Impact of KGD Yield to MCM Failure:

System (MCM) Yield = $(\text{KGD yld}_{\text{comp1}})^{\text{No. of comp1}} \times (\text{KGD yld}_{\text{comp2}})^{\text{No. of comp2}} \times (\text{KGD yld}_{\text{comp3}})^{\text{No. of comp3}}$

Note: A KGD yield of 1.0 means the die is characterized as equal to packaged die in quality, reliability, and performance

Assumptions:

component 1 = ASIC with yield = .75 (2 are used)

Supplied by Vendor A

component 2 = Memory with yield = .88 (4 are used)

Supplied by Vendor B

component 3 = Logic Device with yield = .94 (8 are used)

Supplied by Vendor C

Then System (MCM) Yield = $(0.75)^2 \times (0.88)^4 \times (0.94)^8 = 0.5625 \times 0.599695 \times 0.609569 = 0.205625$

This is a 80% failure rate for the System (MCM)

Using KGD with a yield of >.999 will result in a system failure rate of 1.4%

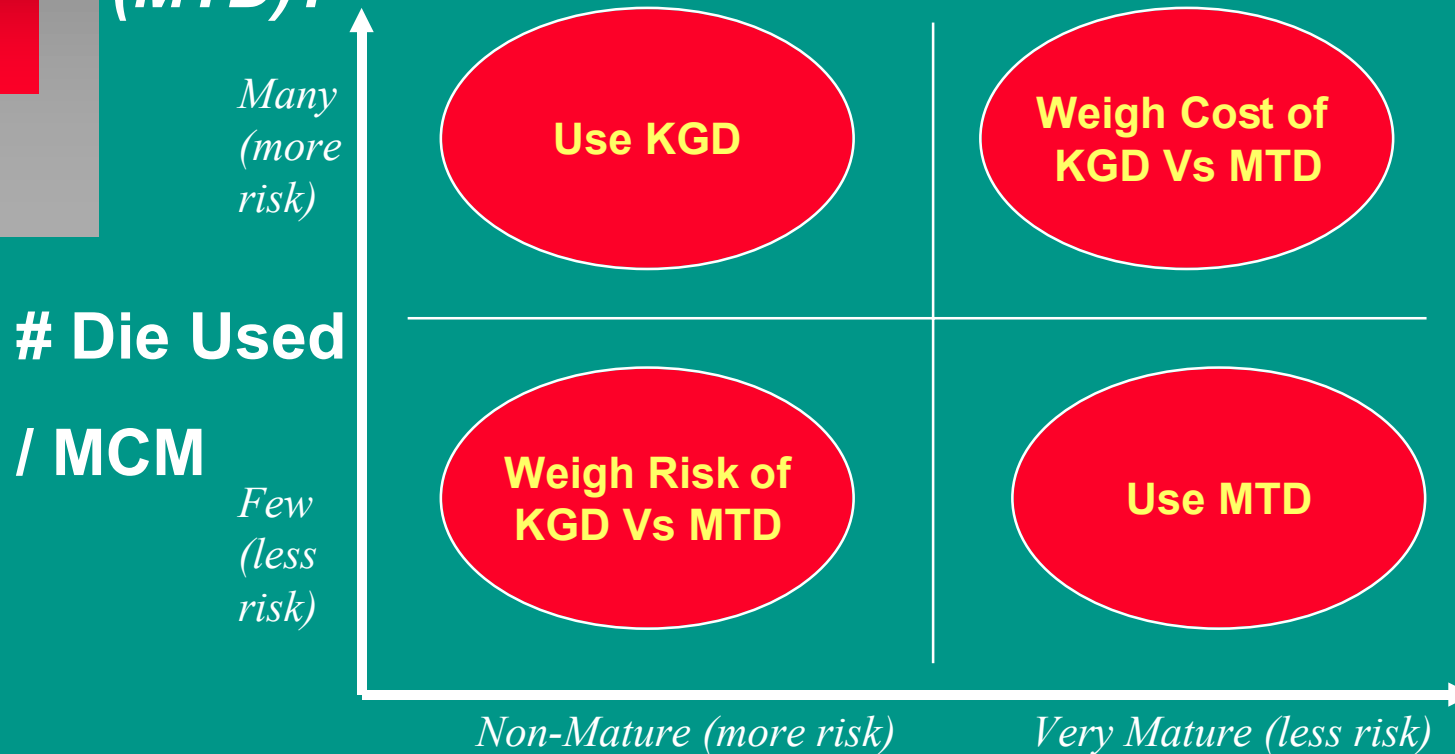
The above calculations assume the quality of MCM die assembly process is = to proven packaged die assemblies.



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When To Use KGD Vs Minimum Tested Die (MTD)? *Rule of Thumb*



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All Information Resides in The JPL COTS Data Base

UTILITIES:

DATA (Parts, Vendors, Surveys, etc.)

INFORMATION (Generic, Plastics, KGD, etc.)

RISK ASSESSMENT (Parts, Technology, etc.)

ANALYSIS (DPA, PCA, SEM, etc.)

TOOLS (Modeling, risk analysis for KGD yield, etc.,)

FORMATS:

PowerPoint

EXCEL

HTML

WORD

PDF



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SUMMARY

Avoiding MCM Risk of Failure:

- Any MCM risk of failure depends on what screening was performed on the die- know the vendor's screening flow options exactly.
- Non-mature die products have the highest risk -especially if procured as bare die or minimum tested die.
- Select types of die product are only reliable if they undergo a dynamic burn-in e.g. memories.
- Speed, temperature, & radiation testing of die are recommended to insure MCM performance.

